UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,221	08/26/2003	Yoshihiro Yamasaki	OKI.567	1912

20987 7590 02/18/2005

VOLENTINE FRANCOS, & WHITT PLLC
ONE FREEDOM SQUARE
11951 FREEDOM DRIVE SUITE 1260
RESTON, VA 20190

EXAMINER	
BARBEE, MANUEL L	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 02/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/647,221	YAMASAKI, YOSHIHIRO	
	Examiner	Art Unit	
	Manuel L. Barbee	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The disclosure is objected to because of the following informalities:

In paragraph 1, the first line of paragraph 1, delete "LSI", and insert --large scale integration (LSI).

Appropriate correction is required.

2. Claims 1 and 8 are objected to because of the following informalities:

In claim 1, line 1 of the claim, delete "LSI", and insert --large scale integration (LSI)--.

In claim 8, line 1 of the claim, delete "5", and insert --7--.

In claim 8, line 2 of the claim, after "second", insert --and--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Sugasawara (US Patent No. 6,043,672).

With regard to a plurality of circuit blocks, as shown in claim 1, Sugasawara teaches an integrated circuit with multiple sections (col. 4, lines 10-20). With regard to a first power supply terminal connected to a first circuit block and a second power supply terminal connected to a second circuit block, as shown in claim 1, Sugasawara teaches

a power connection for each section (col. 4, lines 21-55). With regard to a first level of test voltage for the first circuit block and a second level of test voltage for the second circuit block to test the circuit blocks independently, as shown in claim 1, Sugasawara teaches isolating the sections of the circuit so that they are each powered by an independent power supply for testing (col. 4, line 21 - col. 5, line 26).

With regard to a third circuit block, as shown in claim 5, Sugasawara teaches three sections one region of the integrated circuit (Fig. 1, sections 12, 14, 16). With regard to a switching circuit connected to the first and second power supply terminals and the switching circuit selectively connecting the third circuit block to the first and second power supply terminals, as shown in claim 5, Sugasawara teaches that a single power supply may be used to isolate a defect between two sections (col. 5, lines 14-26). The switches 20 and 22 in Figure 1 of Sugasawara could be manipulated to connect section 14 to the voltage terminal of section 12 or the voltage terminal of section 16 while keeping sections 12 and 16 isolated with different voltage levels.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2, 3, 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugasawara in view of Rostoker et al. (US Patent No. 5,489,538).

Sugasawara teaches all the limitations of claim 1 upon which claims 2 and 3 depend and claim 5 upon which claims 6 and 7 depend. Further with regard to connecting the circuit blocks and terminals one-by-one and connecting to a common external terminal after the tests are completed, as shown in claims 3 and 7, Sugasawara teaches a step for connecting and isolating each section of the circuit and connecting to one common power terminal during normal operation (col. 4, lines 21-55).

Sugasawara does not teach testing the circuit blocks on a wafer before fabrication, as shown in claims 2, 3, 6 and 7. Rostoker et al. teach forming test points and testing a wafer prior to completing the fabrication process (col. 10, lines 6-55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the integrated circuit testing device, as taught by Sugasawara, to include testing the devices before fabrication is completed, as taught by Rostoker et al., because then failed chips could have been repaired before fabrication was completed (Rostoker et al., col. 1, line 65 - col. 2, line 5).

7. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugasawara in view of Rostoker et al. as applied to claims 3 and 7 above, and further in view of Kokado (US Patent No. 5,072,274).

Sugasawara and Rostoker et al. teach all the limitations of claim 3 upon which claim 4 depends and claim 7 upon which claim 8 depends. Sugasawara and Rostoker et al. do not teach that the supply terminals of the circuit blocks are connected to the common external terminal in a wire-bonding process, as shown in claims 4 and 8. Kokado teaches connecting package leads for supplying power using wire bonding (col.

6, lines 22-41). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the integrated circuit testing combination, as taught by Sugasawara and Rostoker et al., to include wire bonding the external power supply leads, as taught by Kokado, because then the power supply would have been well connected.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ohno et al. (US Patent No. 4,255,672) teaches a large scale semiconductor which connects different parts of the circuit with different power supply levels of voltage.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Manuel L. Barbee whose telephone number is 571-272-2212. The examiner can normally be reached on Monday-Friday from 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on 571-272-2216. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

mlb
February 14, 2005

MARC S. HOFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800